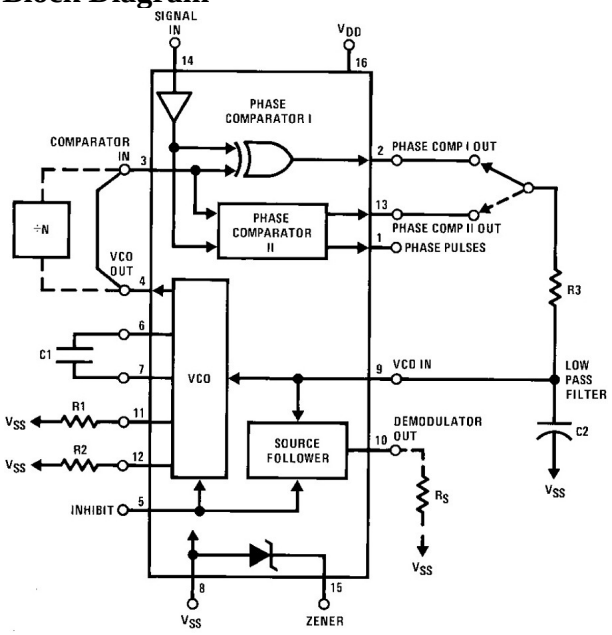
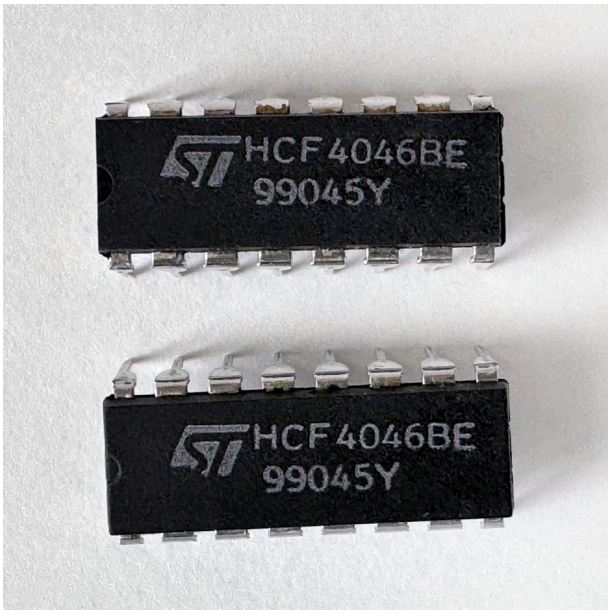
HCF4046B
CMOS Micropower Phase-Locked Loop Macro Model

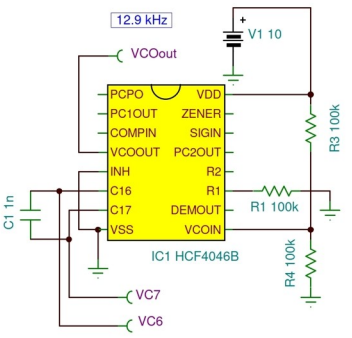
Block Diagram

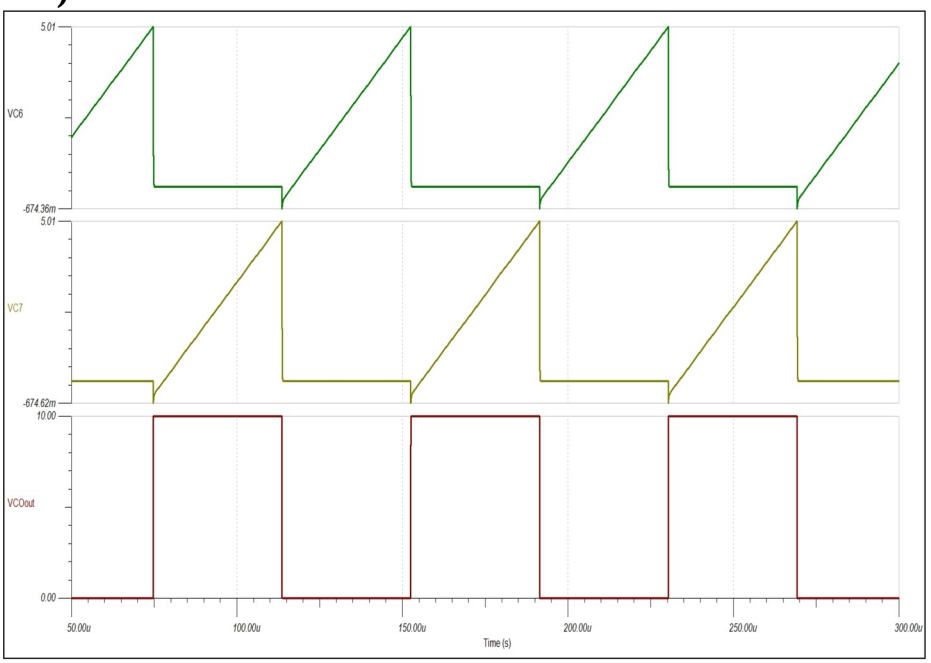


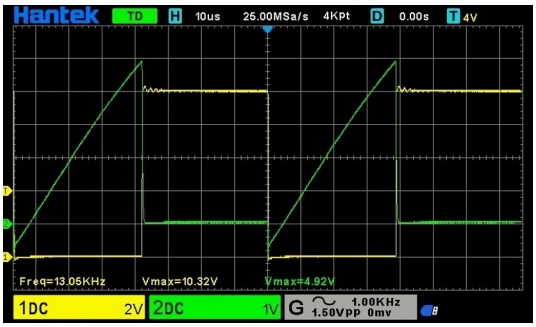


This model is valid for the following devices (within max. ratings): CD4046BM/CD4046BC. (The HCF4046B has a maximum supply voltage of 22 V and an operating voltage of 3–20 V.)

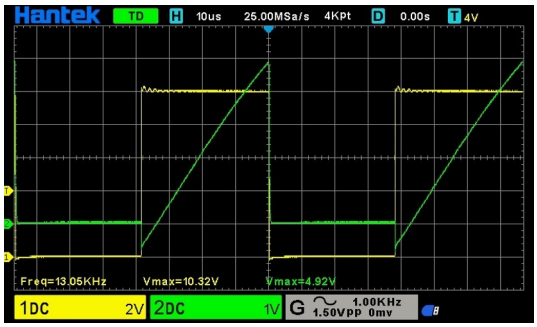
VCO Test Circuit (R2 = ∞)





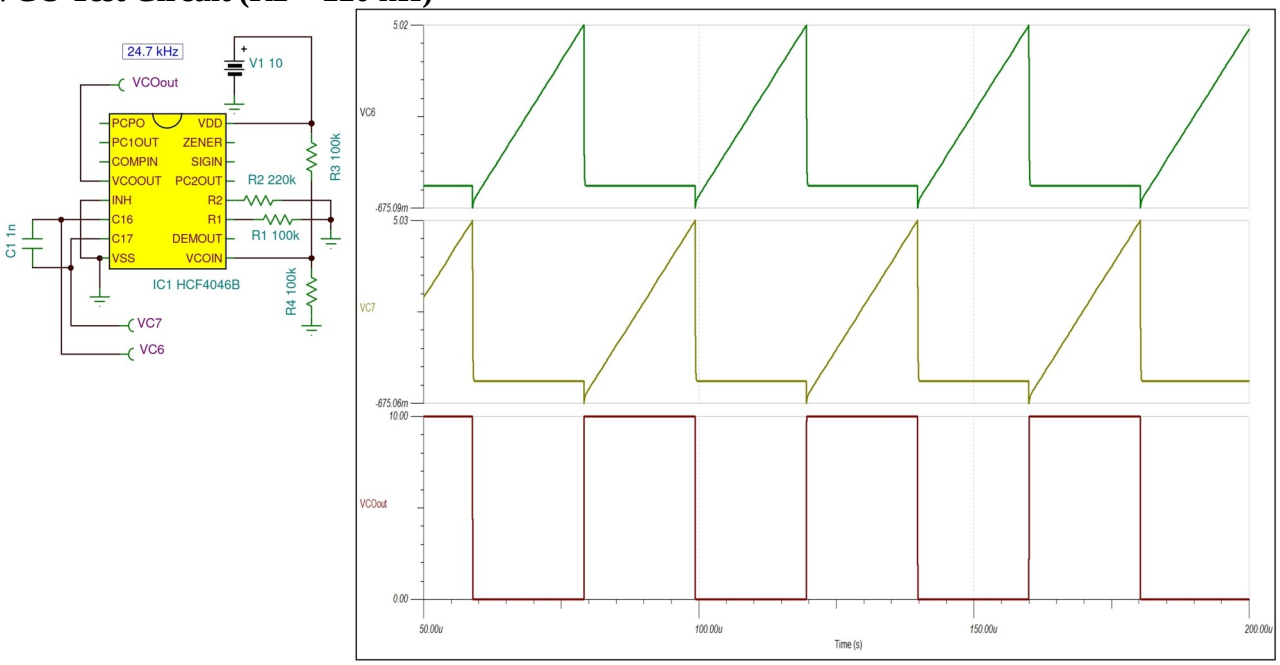


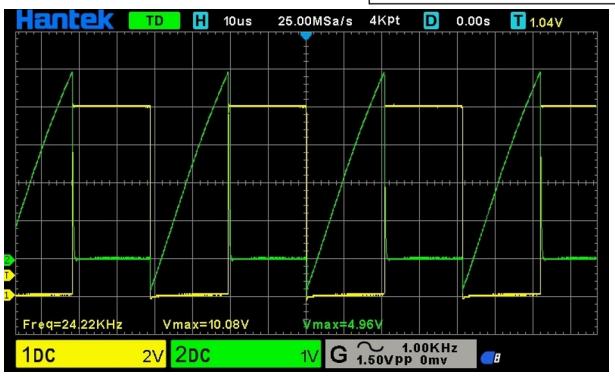
VCOout and VC6



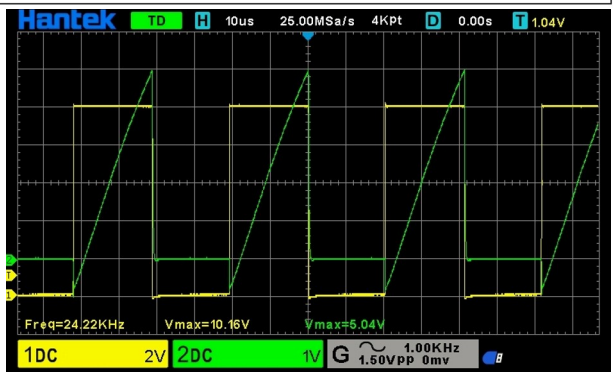
VCOout and VC7

VCO Test Circuit (R2 = 220 kΩ)



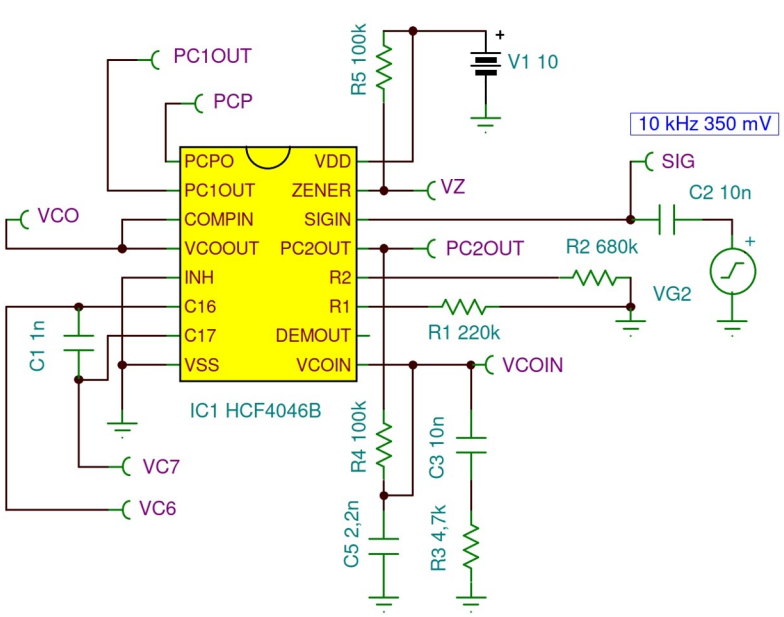


VCOout and VC6



VCOout and VC7

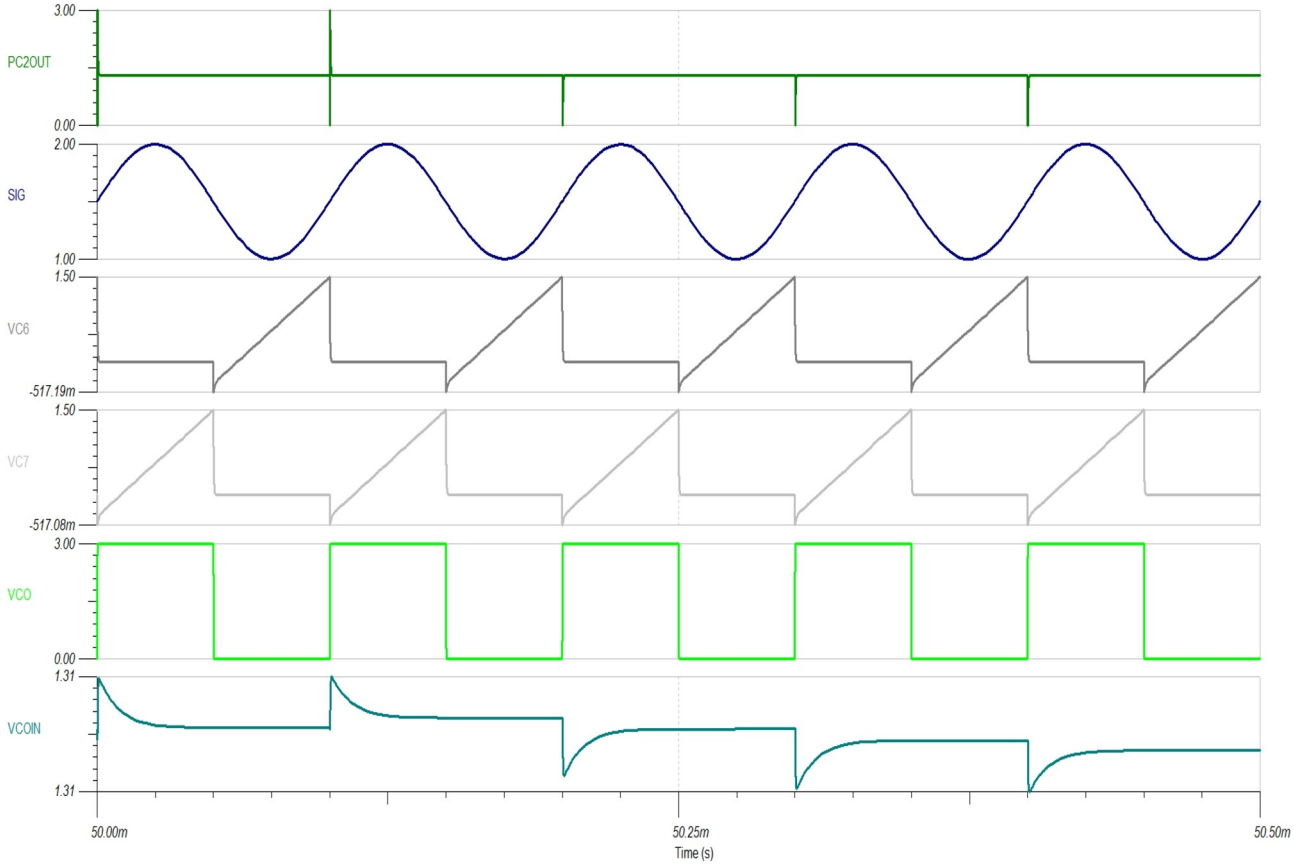
The circuit below provides guidance for determining the approximate values of the external components of the HCF4046B in a 10 kHz phase-locked loop system.



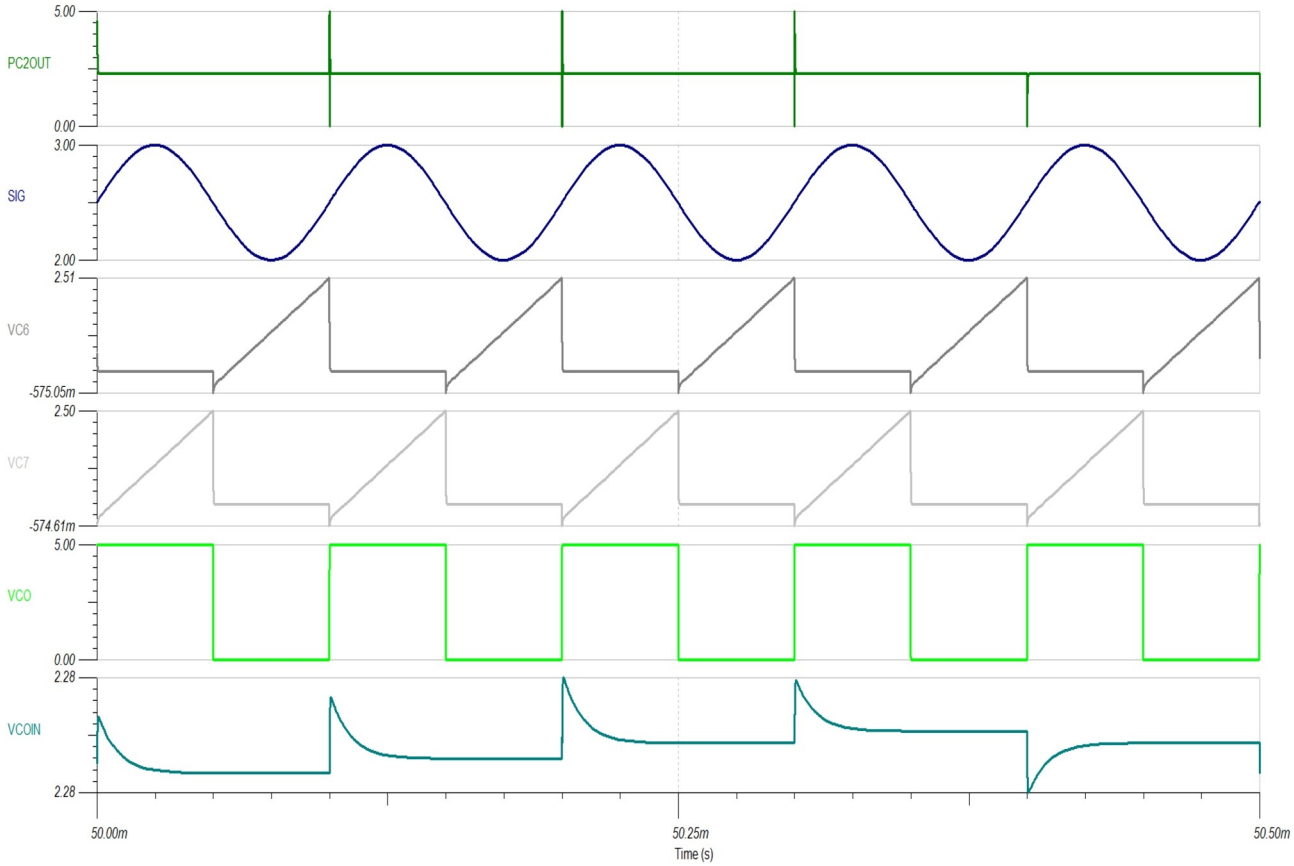
VDD R1	R2
3 V 80 k	680k
5 V 150 k	680k
10 V 220 k	680k
15 V 180 k	1MEG
20 V 220 k	1MEG

AC test circuit for different supply voltages.

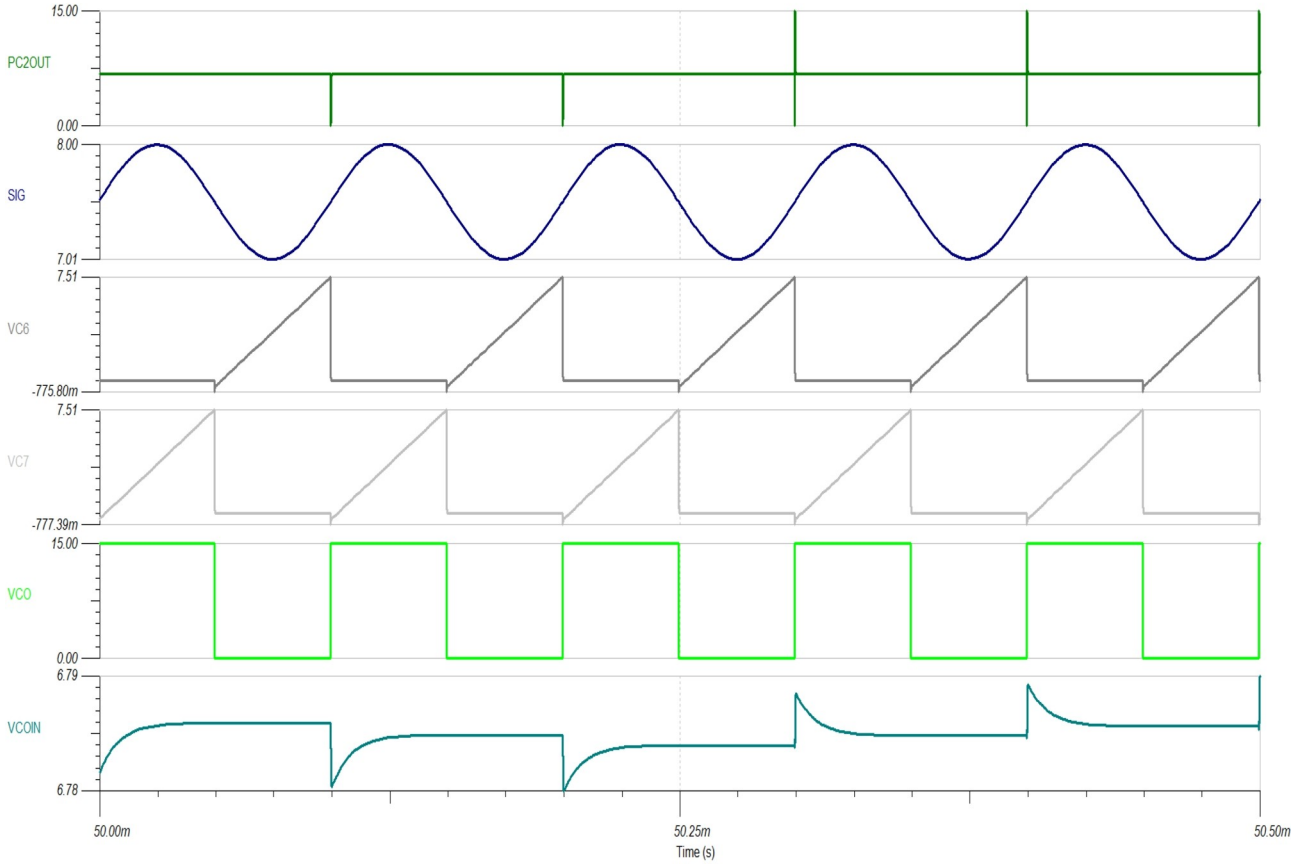
VDD= 3 V


3.00
PC2OUT
0.00
2.00
SIG
1.00
1.50
VC6
-517.19m
1.50
VC7
-517.08m
3.00
VCO
0.00
1.31
VCOIN
1.31
50.00m
50.25m
50.50m
Time (s)

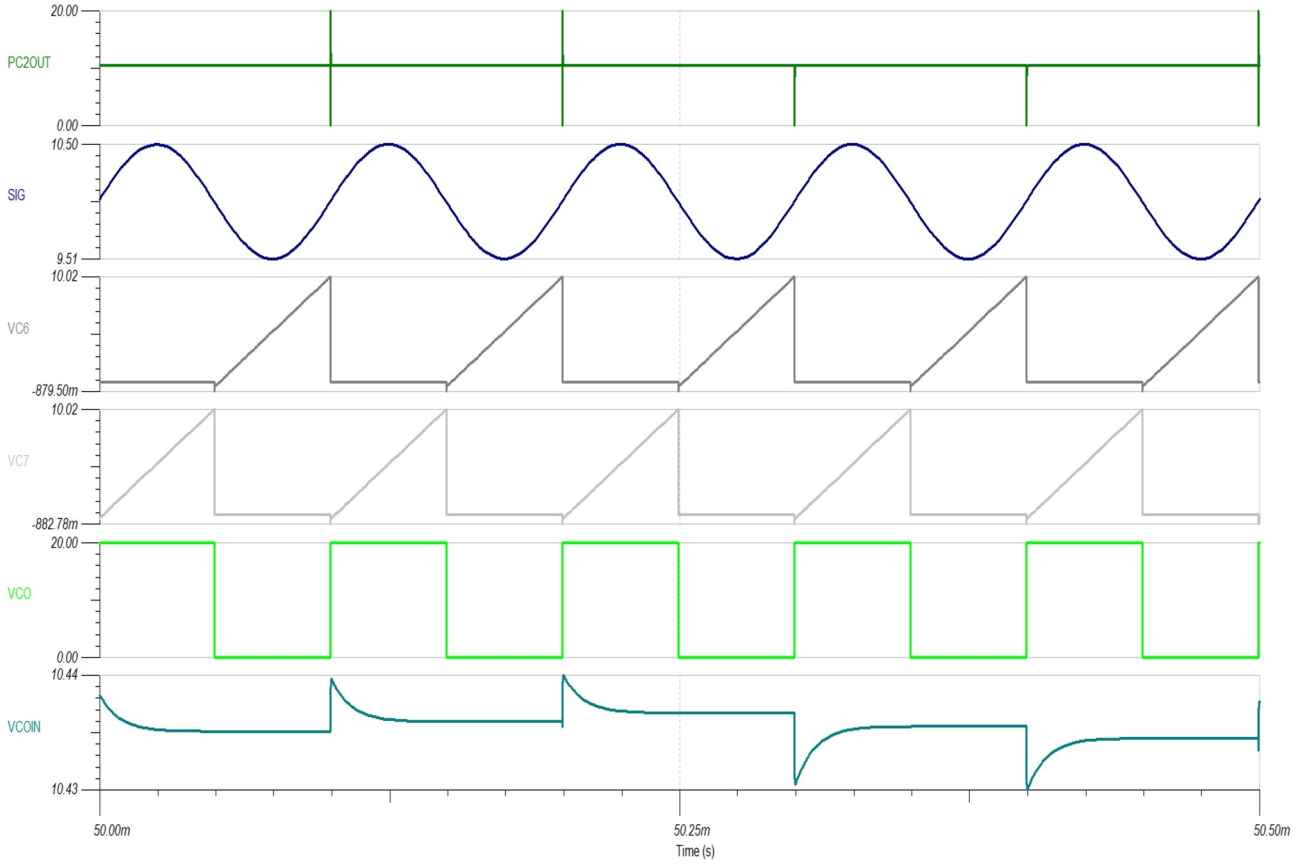
VDD= 5 V


5.00
PC2OUT
0.00
3.00
SIG
2.00
2.51
VC6
-575.05m
2.50
VC7
-574.61m
5.00
VCO
0.00
2.28
VCOIN
2.28
50.00m
50.25m
50.50m
Time (s)

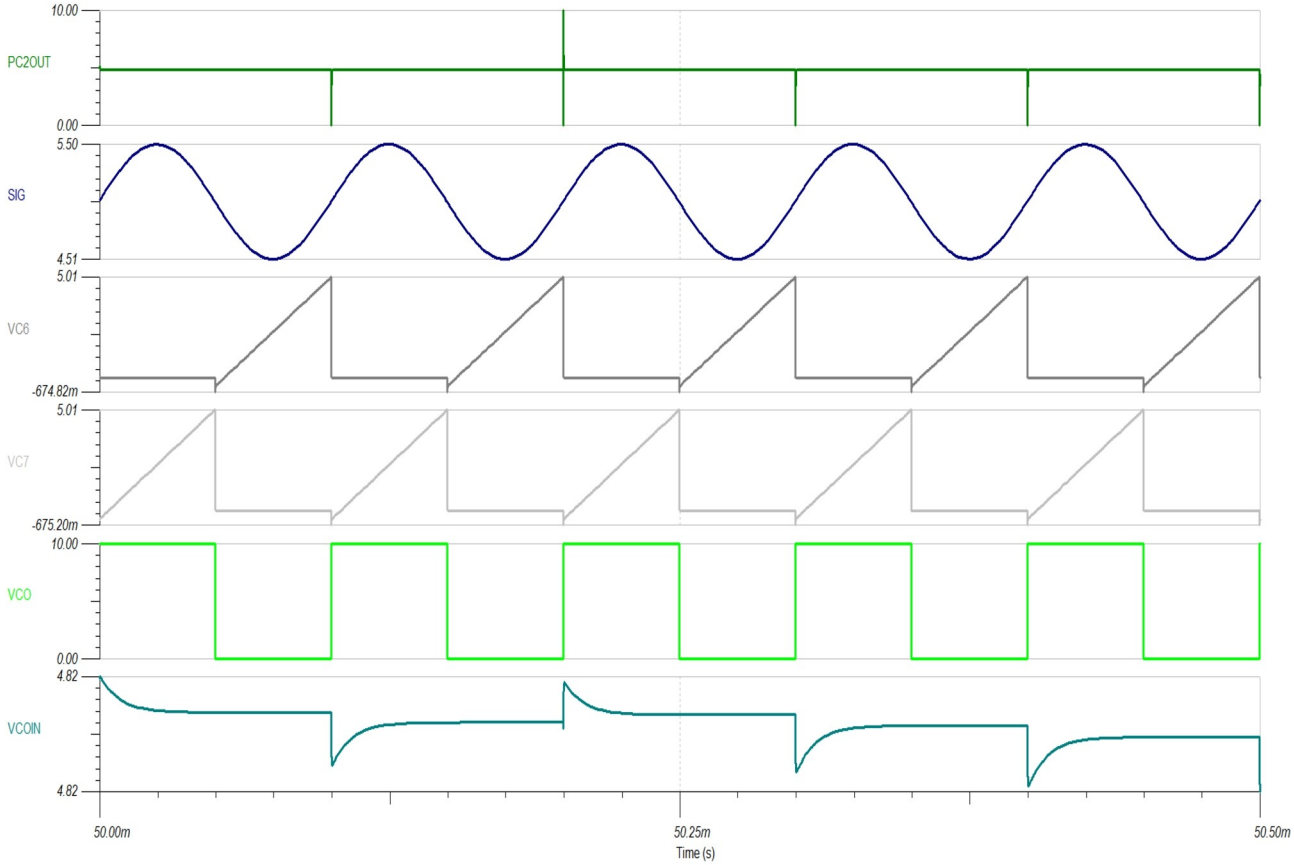
VDD= 15 V



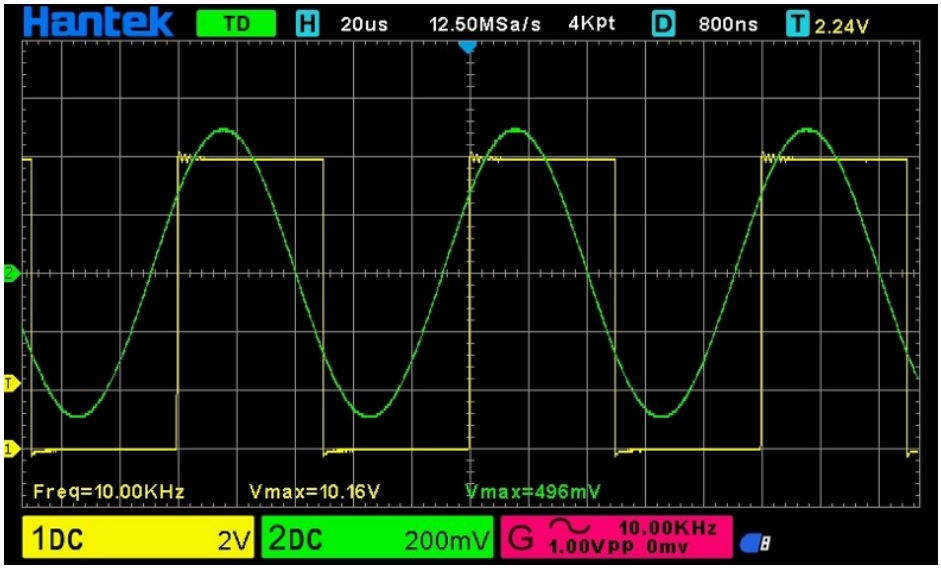
VDD= 20 V



VDD= 10V

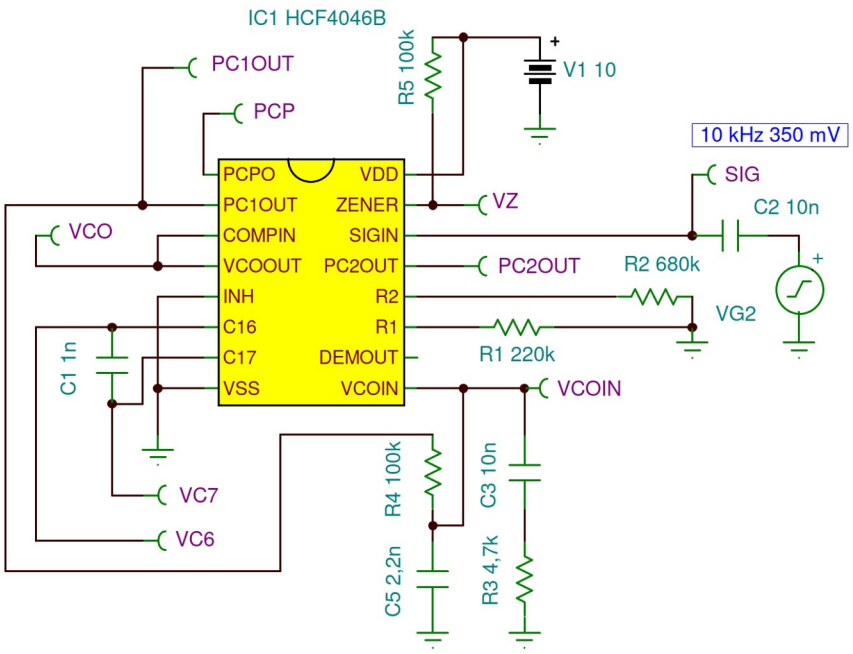


Real device VDD= 10 V (VCO and SIG)



Phase Comparator I is implemented as an exclusive-OR network, operating analogously to an overdriven balanced mixer. To maximize the lock range, both the signal and comparator input frequencies must maintain a 50% duty cycle. The phase angle between the signal and the comparator input varies from 0° to 180°, with 90° corresponding to the center frequency. Typical waveforms of a CMOS phase-locked loop employing Phase Comparator I in the locked condition at f_0 are shown on the following page.

Phase Comparator I Characteristics



VDD	R1	R2
3 V	80 k	680k
5 V	150 k	680k
10 V	220 k	680k
15 V	180 k	1MEG
20 V	220 k	1MEG

VDD= 10 V