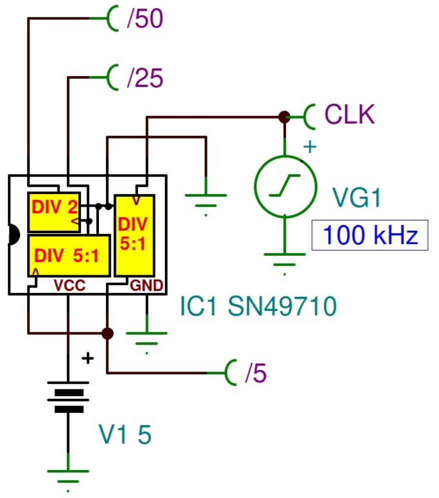
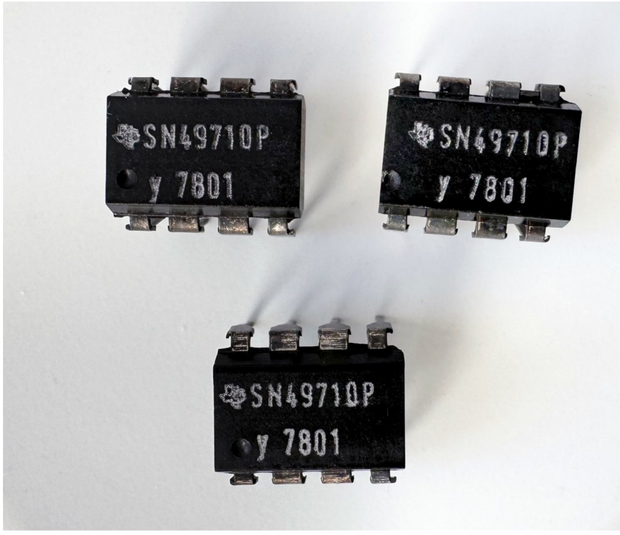
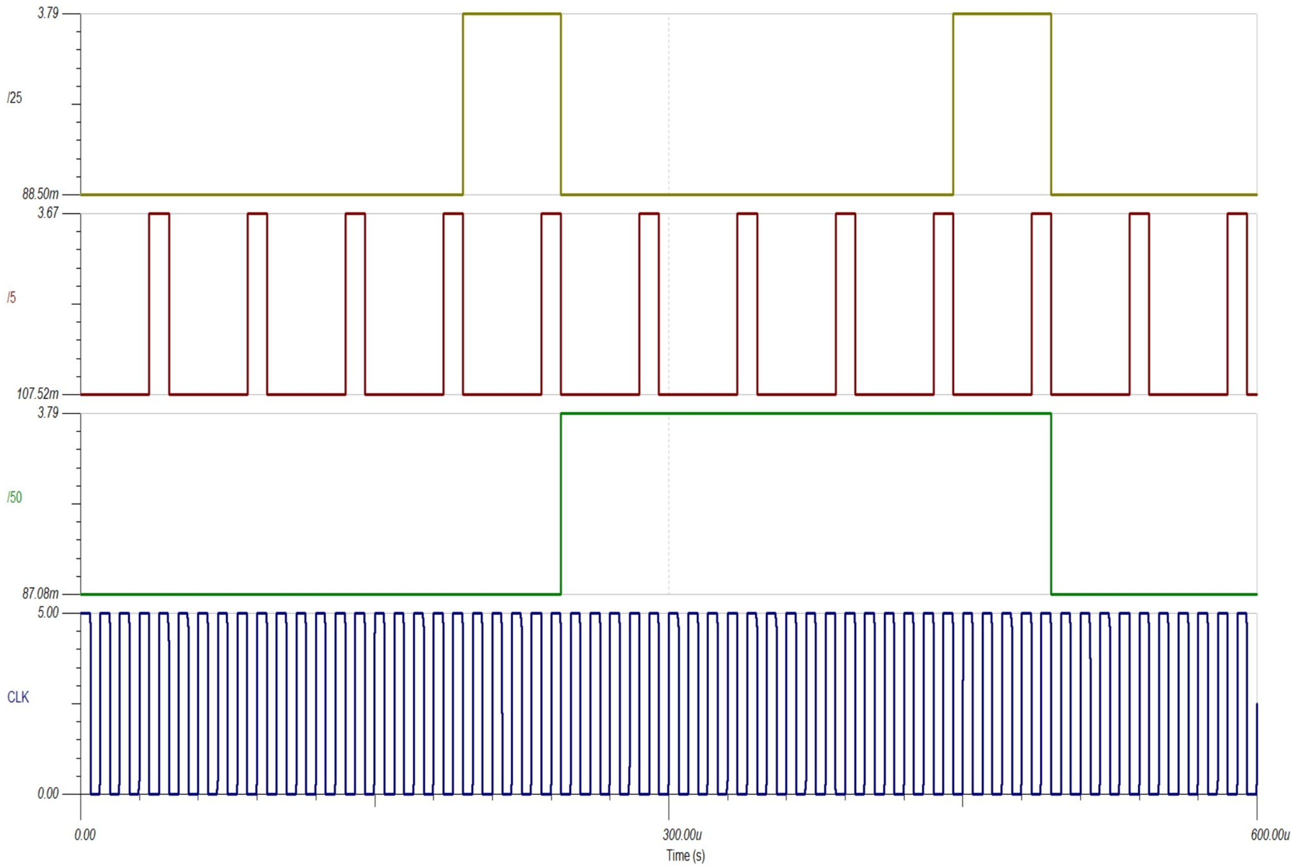
SN49710 TTL Frequency Divider 50:1 Macro Model

Typical Characteristics

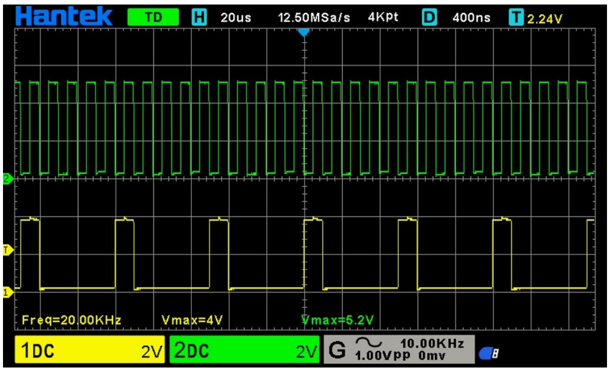




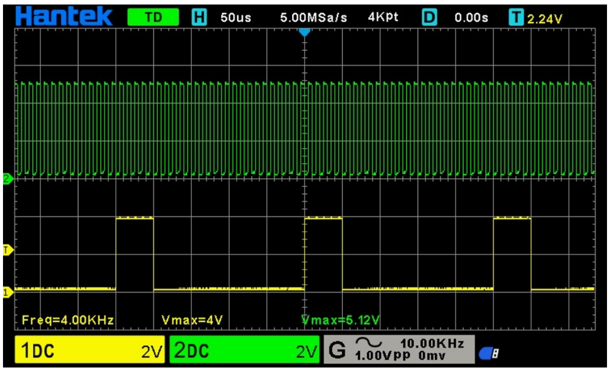
Originally, it was designed to derive a 1 Hz signal by dividing the mains frequency, serving as a timing reference for digital clocks operating on mains power.



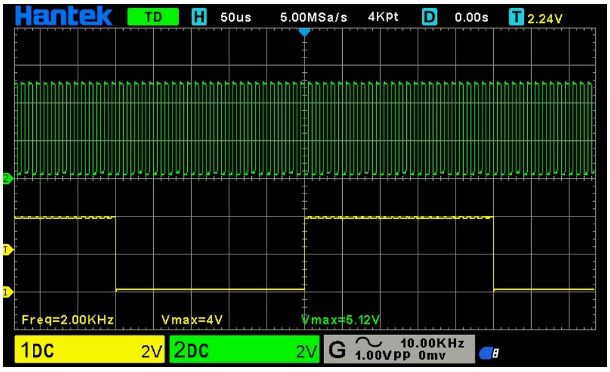
It contains negative-edge-triggered counters with an asynchronous (active-high) reset. Supported division ratios include 5:1, 10:1, 25:1, and 50:1.



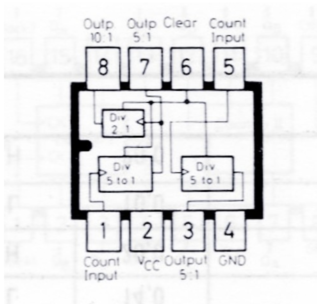
5:1



25:1



50:1



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