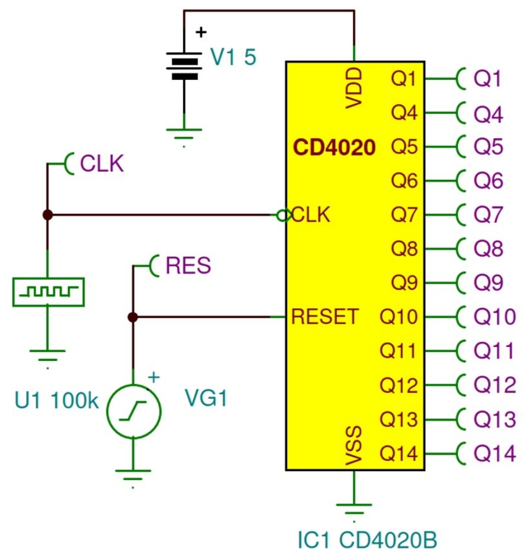
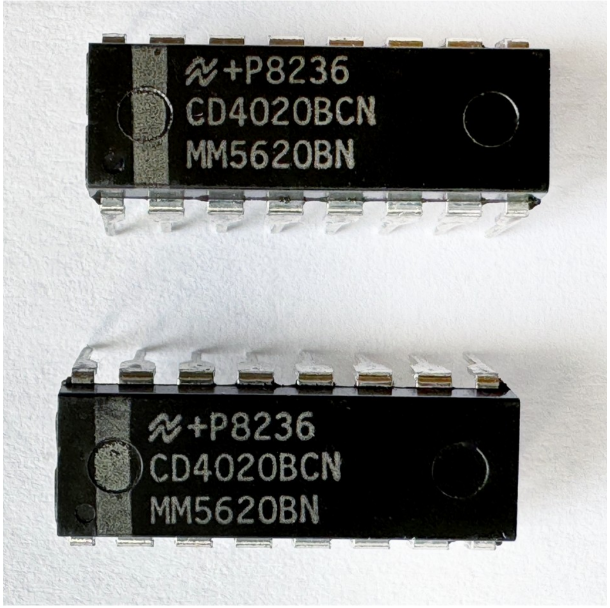
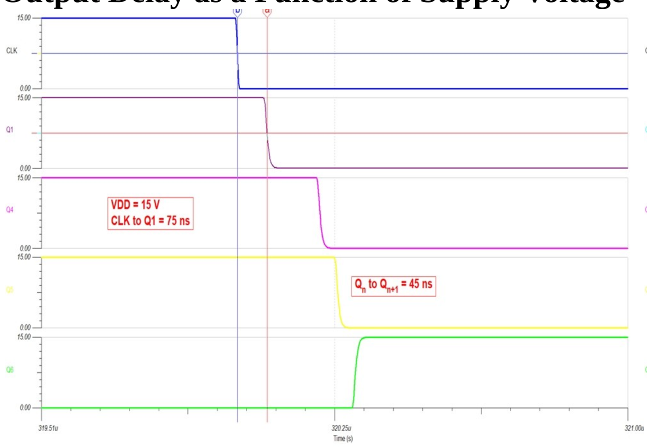
CD4020B 14-Bit Binary Counter Macro Model

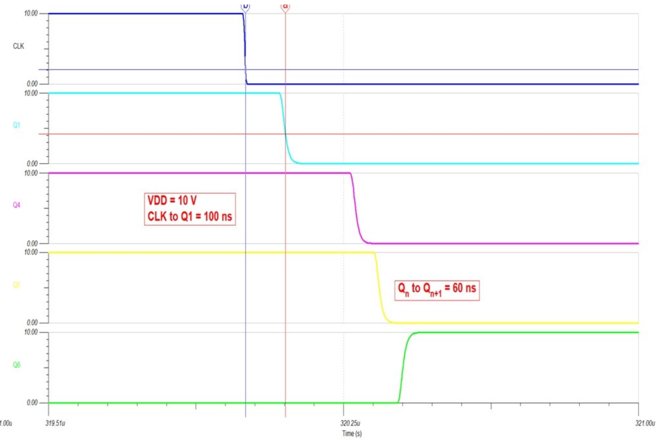
Test Circuit

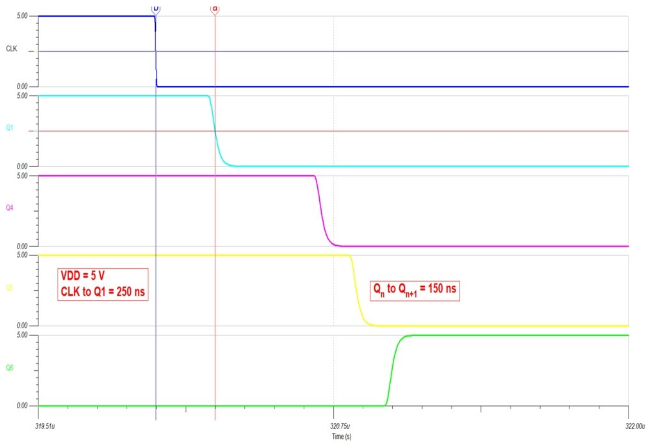


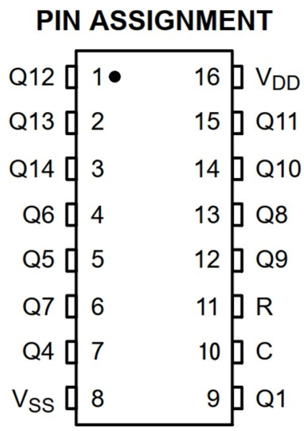


Output Delay as a Function of Supply Voltage



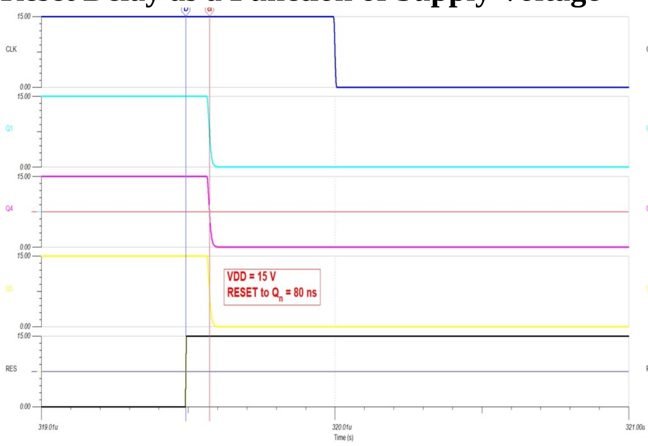


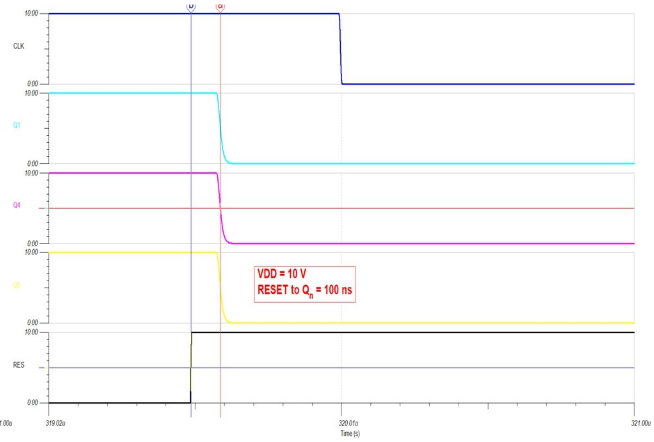


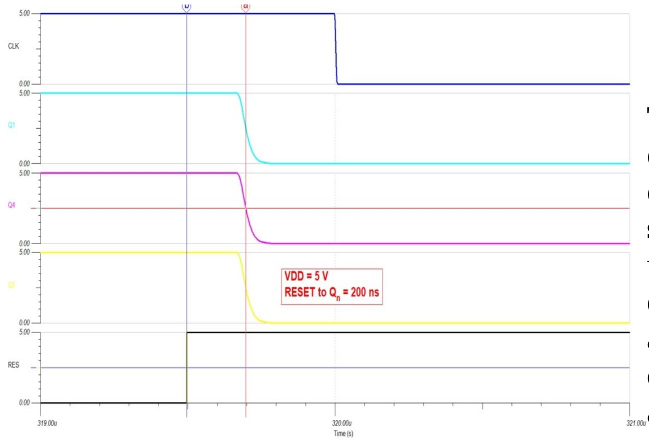


The device advances the count on the negative-going edge of the clock pulse. Its clock input circuit features Schmitt trigger action, which provides pulse shaping and enables the device to accept clock input pulses with unlimited rise and fall times. The counters are reset to the zero state by a logical "1" at the reset input independent of clock. State changes of the Q_n outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with CLK of the CD4020B.

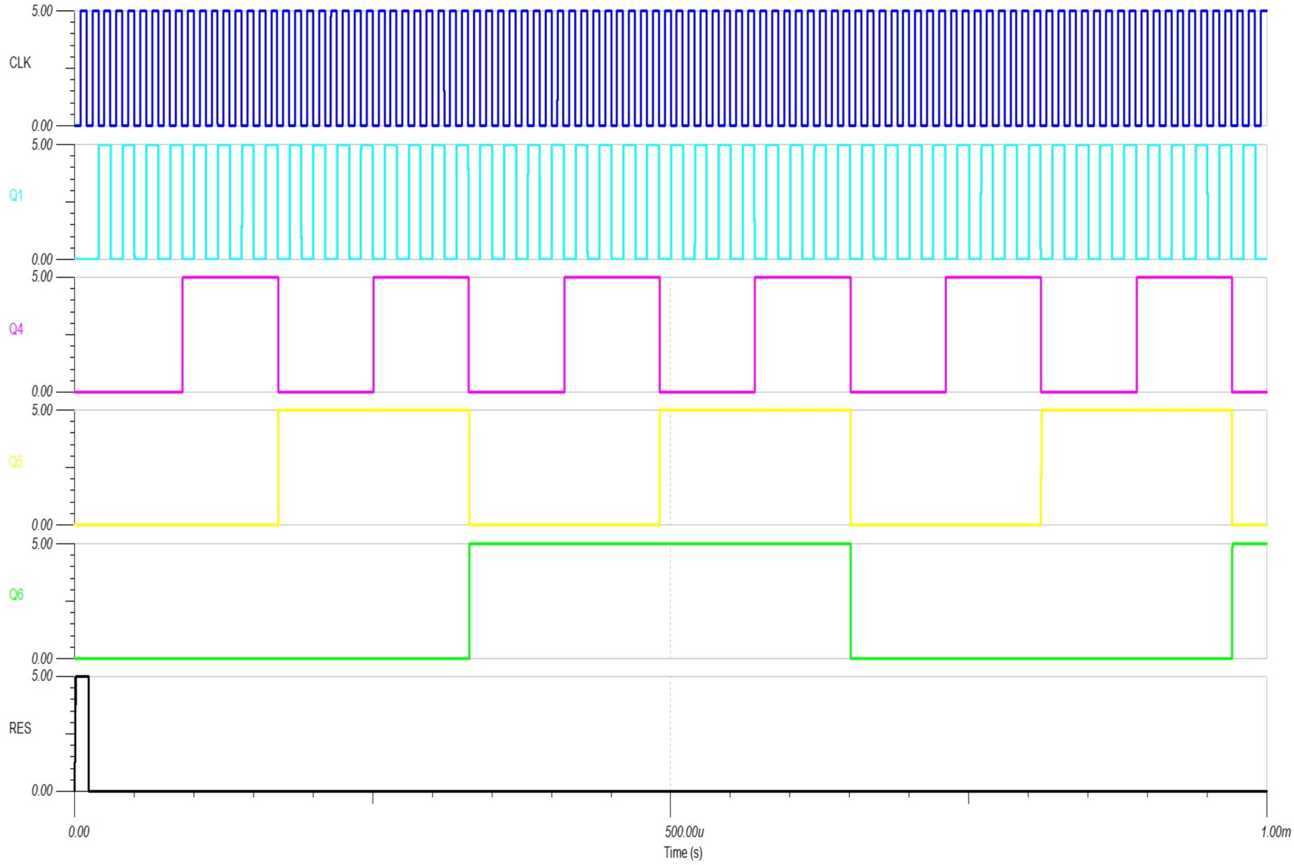
Reset Delay as a Function of Supply Voltage

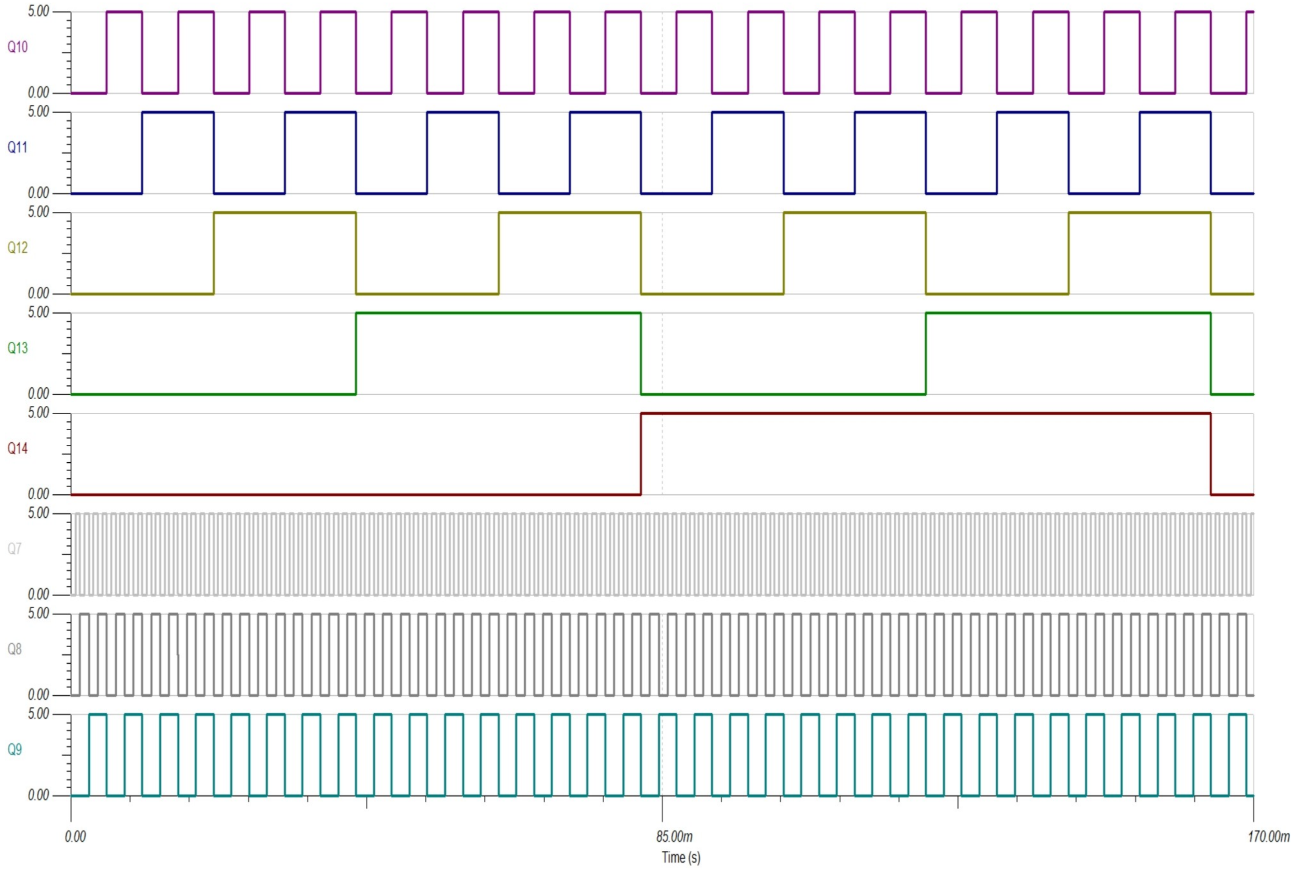






To enhance clarity, the complex diagrams are divided into two segments. The counter is driven by a 100 kHz clock signal, and the simulation duration is set to 170 ms. This timeframe ensures comprehensive validation of all output states. Since the outputs are analog CMOS circuits, the process takes a considerable amount of time. However, this approach allows us to observe the exact voltage at each output under load conditions.




5.00
Q10
0.00
5.00
Q11
0.00
5.00
Q12
0.00
5.00
Q13
0.00
5.00
Q14
0.00
5.00
Q7
0.00
5.00
Q8
0.00
5.00
Q9
0.00
0.00
85.00m
170.00m
Time (s)

Zabb Csaba