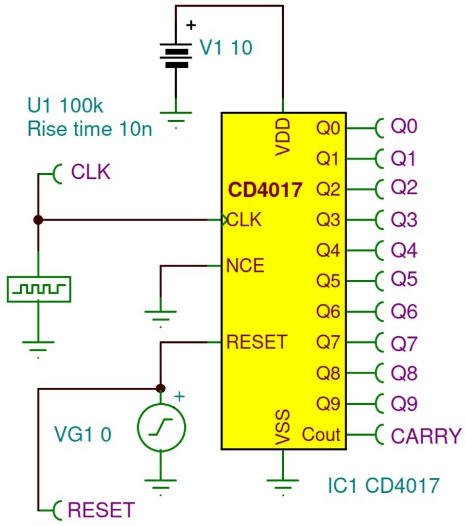
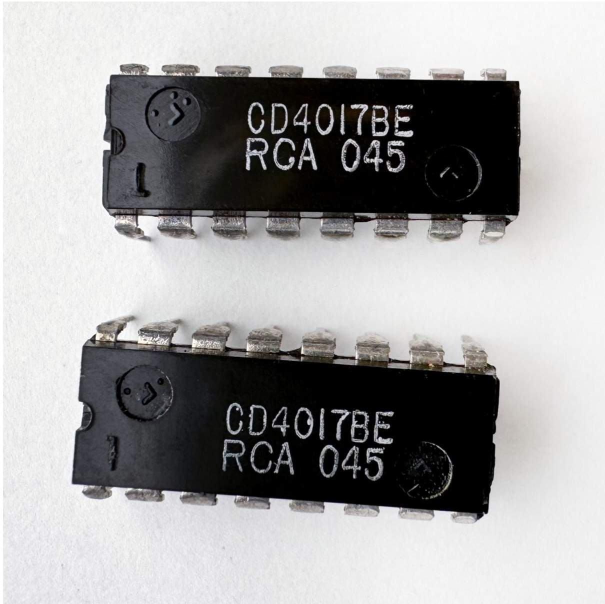
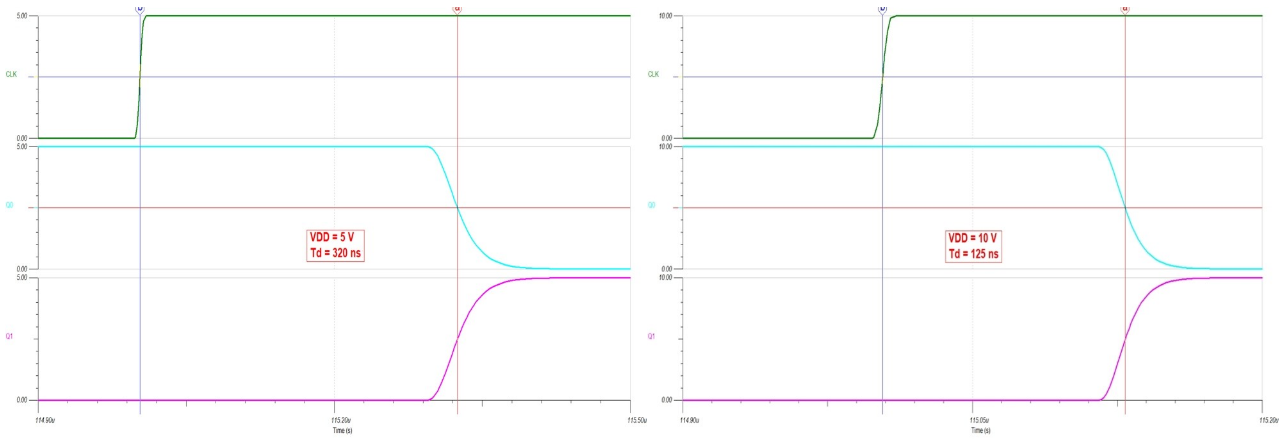
CD4017 Decade Counter/Divider with 10 Decoded Outputs Macro Model

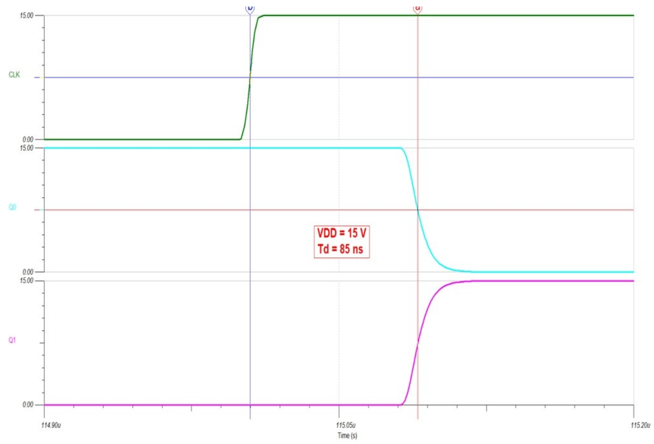
Test Circuit

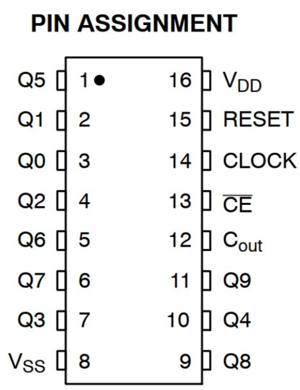




Output Delay as a Function of Supply Voltage

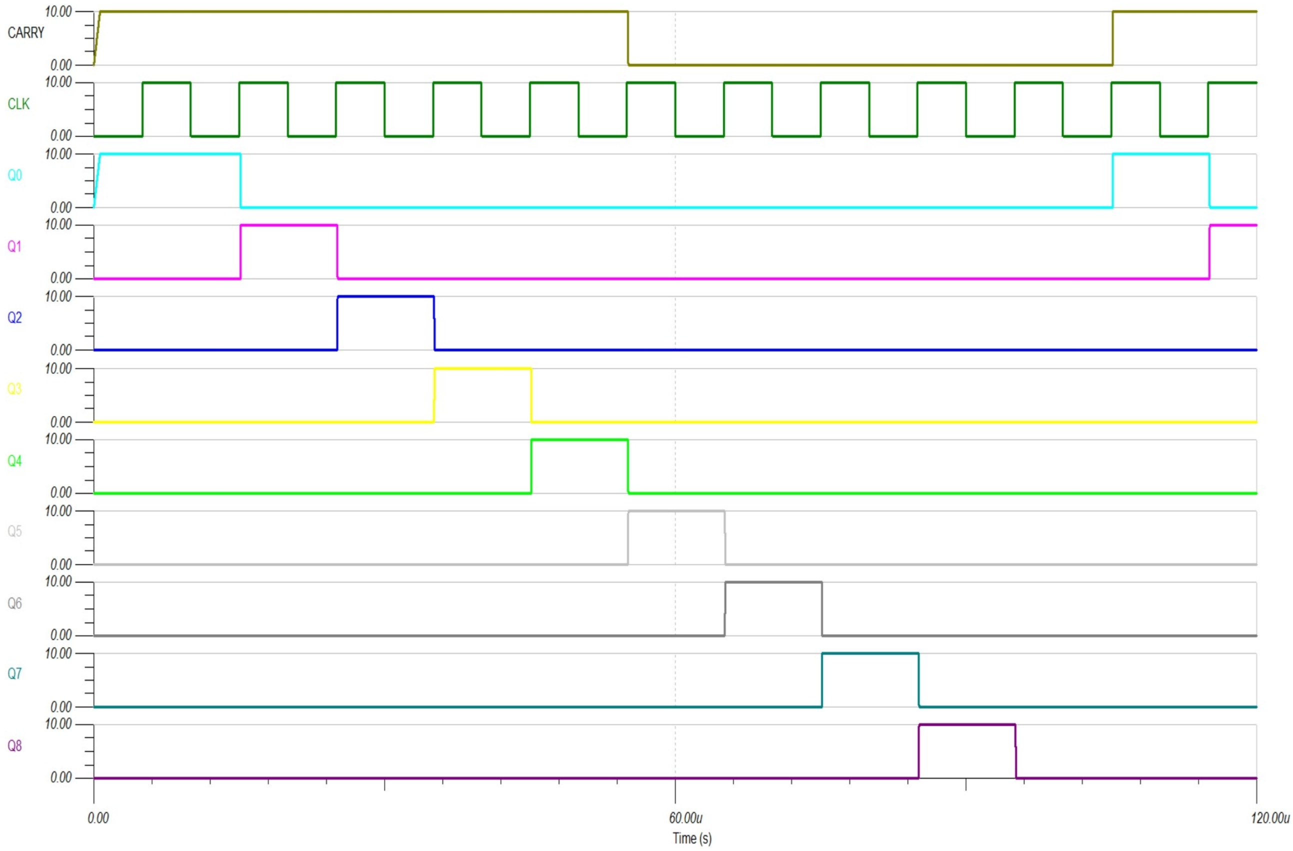


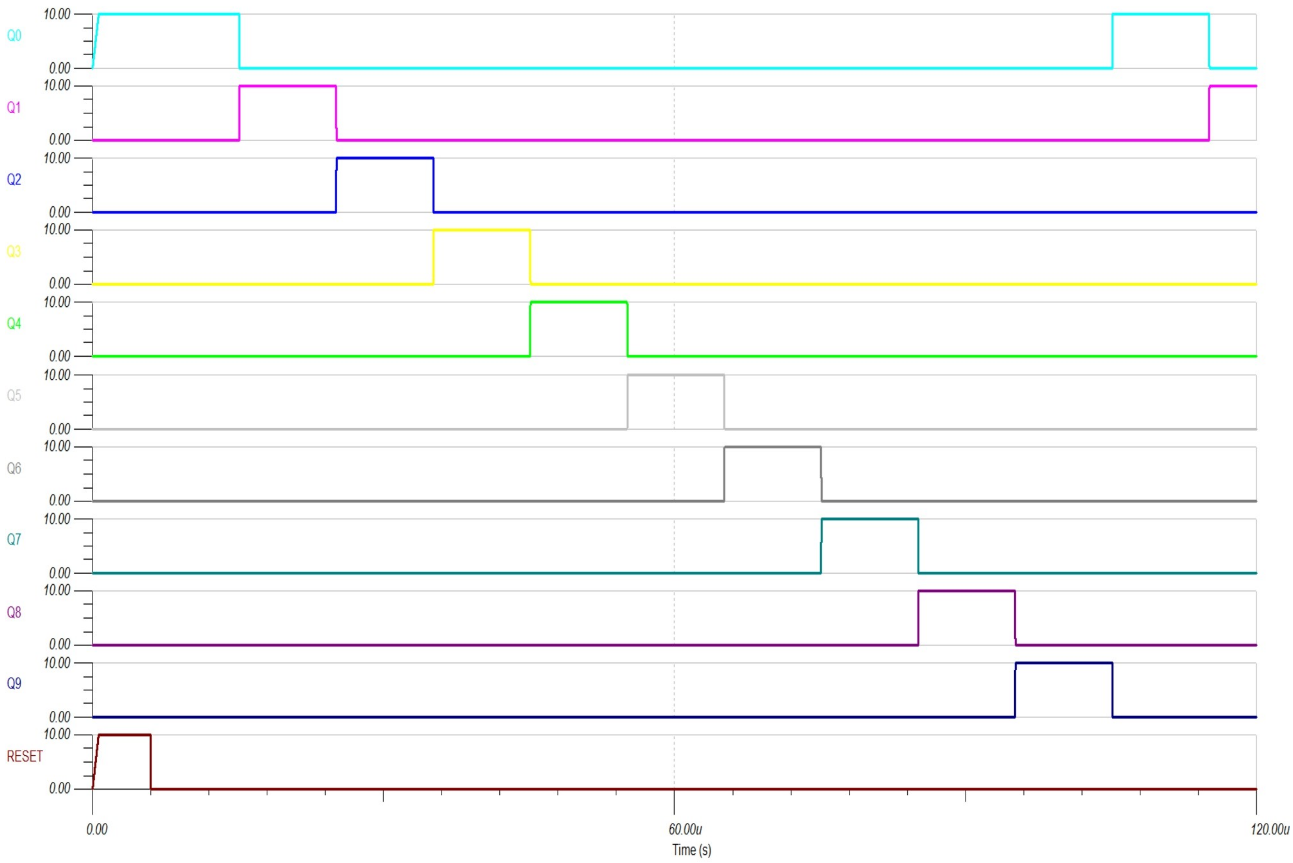




To enhance clarity, the complex diagrams are divided into two segments. The counter is driven by a 100 kHz clock signal, and the simulation duration is set to 120 µs. This timeframe ensures comprehensive validation of all output states.

The outputs utilize analog CMOS technology, allowing for detailed analysis of their load behavior under simulated conditions.

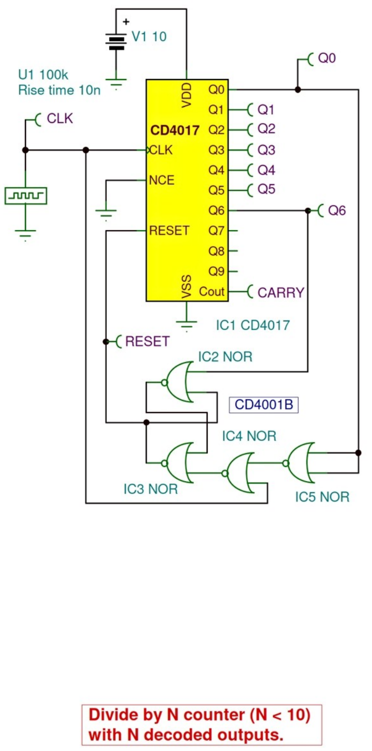


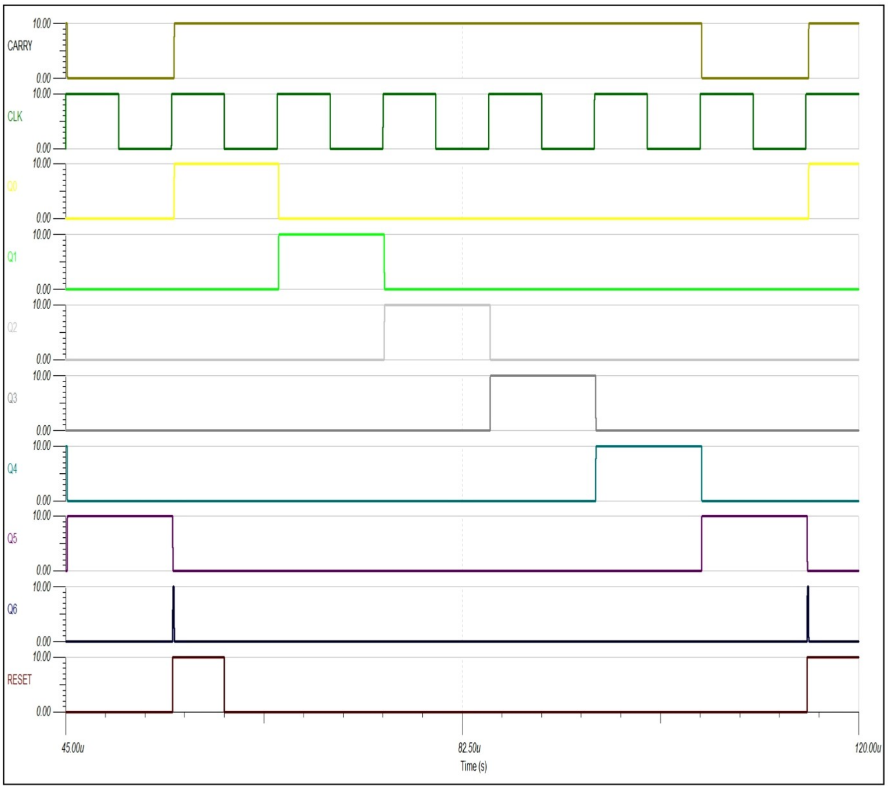


The CD4017 is a five-stage Johnson decade counter with an integrated code converter.
Its clock input circuit features Schmitt trigger action, which provides pulse shaping and enables the device to accept clock input pulses with unlimited rise and fall times.

Divide-by-N Counter (N ≤ 10) with N Decoded Outputs

A digital counter circuit that divides the input clock frequency by an integer N (where N is less than or equal to 10), and provides N individual decoded outputs—each corresponding to one of the N count states.





When the Nth decoded output of the CD4017 is activated (i.e., on the Nth clock pulse), an S-R flip-flop—constructed from two NOR gates of the CD4001B—generates a reset pulse. This pulse clears the CD4017 counter, returning it to its zero state.
The flip-flop is reset when the clock signal is low and the decoded "0" output of the CD4017 is high. This coincidence re-enables the CD4017, allowing it to resume counting from zero.

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