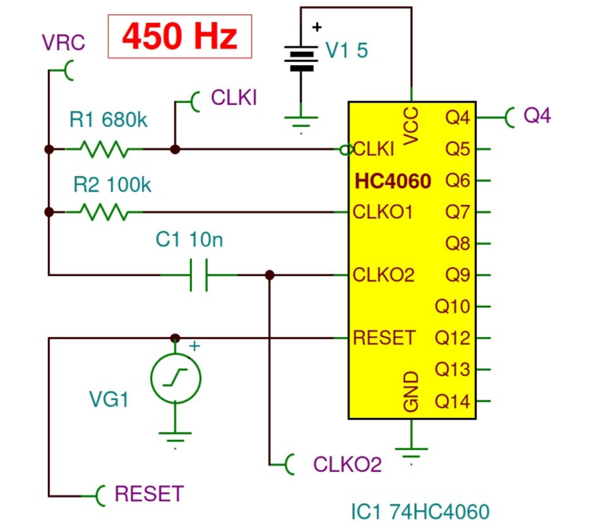
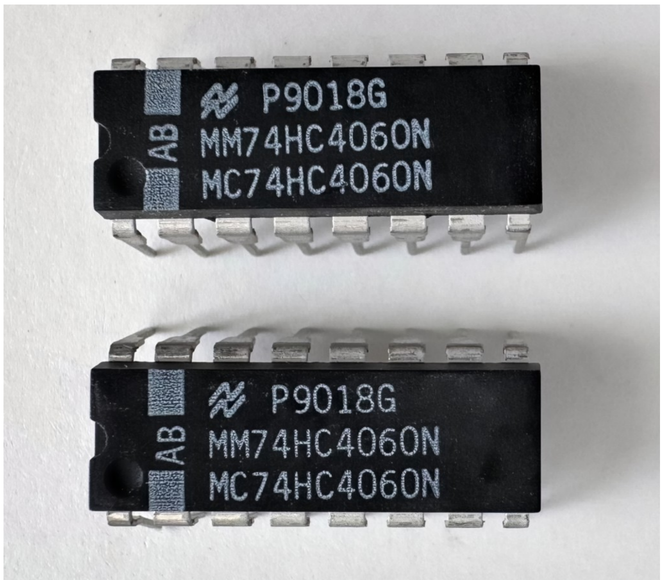
MM74HC4060 14-Stage Binary Ripple Counter With Oscillator Macro Model

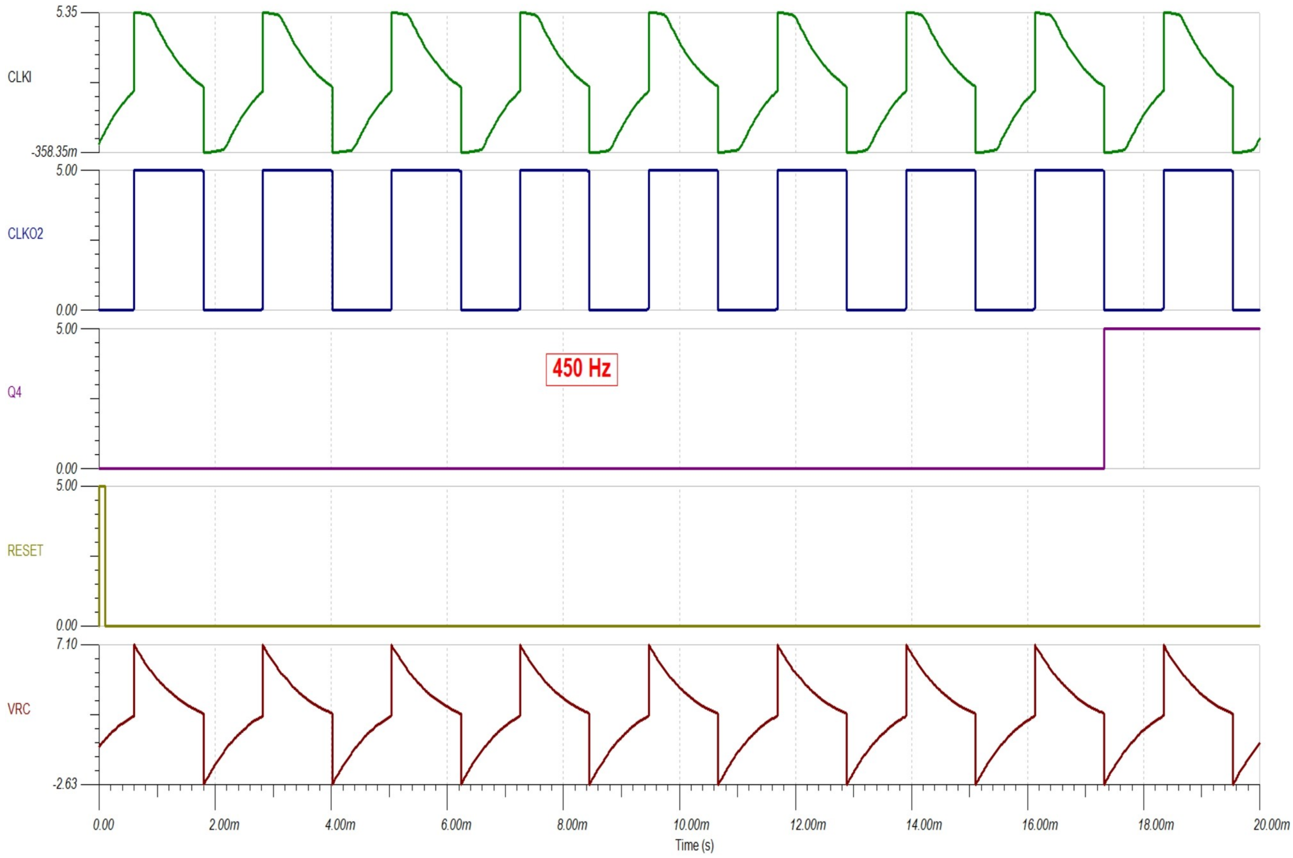
Oscillator Circuit Using RC Configuration



$$f \approx \frac{1}{2.2\,R_2 C_1} \quad \text{(f in Hz, } R_2 \text{ in ohms, } C_1 \text{ in farads)}$$

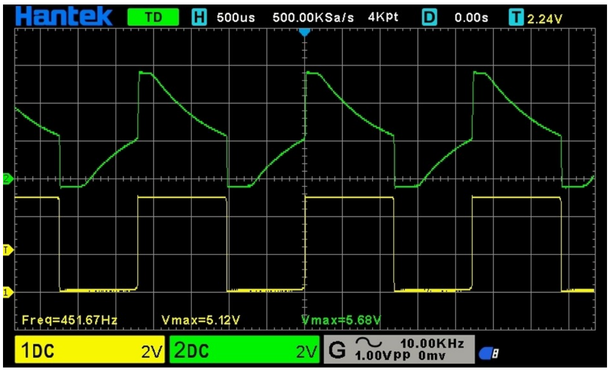


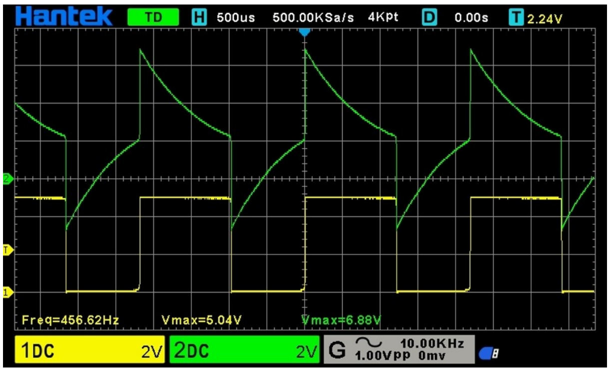
Simulation result of RC oscillator circuit



The signal propagation delay from CLKI to Q4 is 43 ns.

The signals measured with the oscilloscope on the device are shown on the following page. The simulated and measured frequencies match closely.

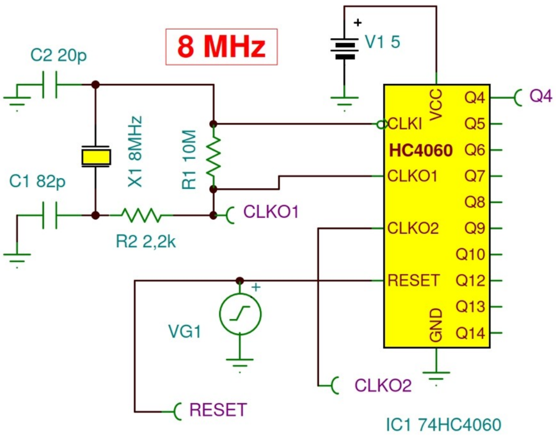


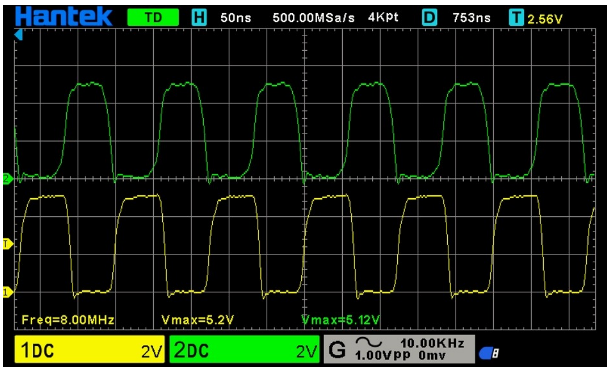


CLKO2 and CLKI **CLKO2 and VRC**

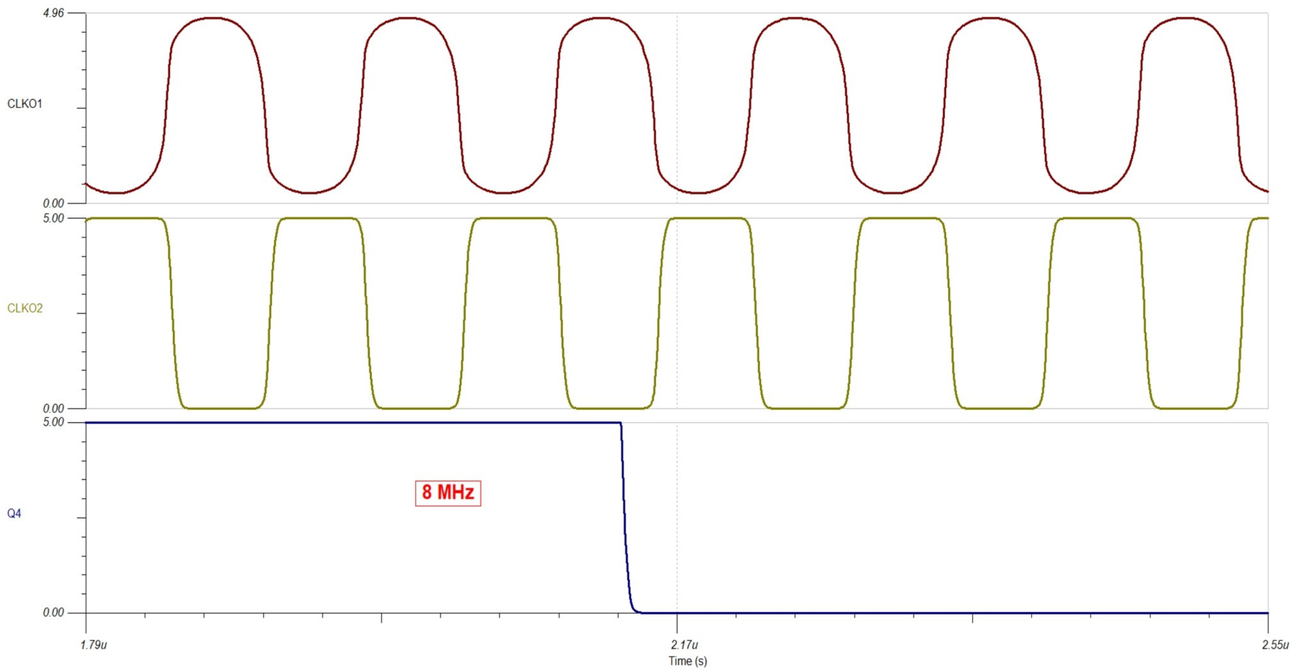
The oscilloscope's load slightly affects the frequency at high-impedance nodes.

Pierce Crystal Oscillator Circuit



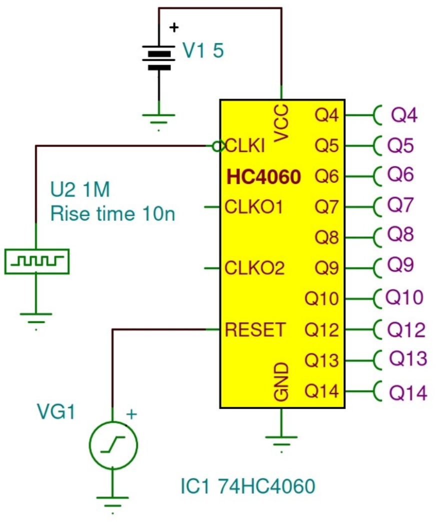


CLKO2 and CLKO1



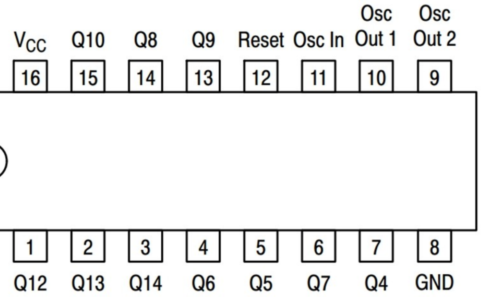
Next, we will use an external oscillator operating at 1 MHz. The 18 ms simulation analyzes all outputs. Since the outputs are analog CMOS circuits, the process takes a considerable amount of time. However, this approach allows us to observe the exact voltage at each output under load conditions. The propagation delay between consecutive outputs (Q_n to Q_{n+1}) is 9 ns.

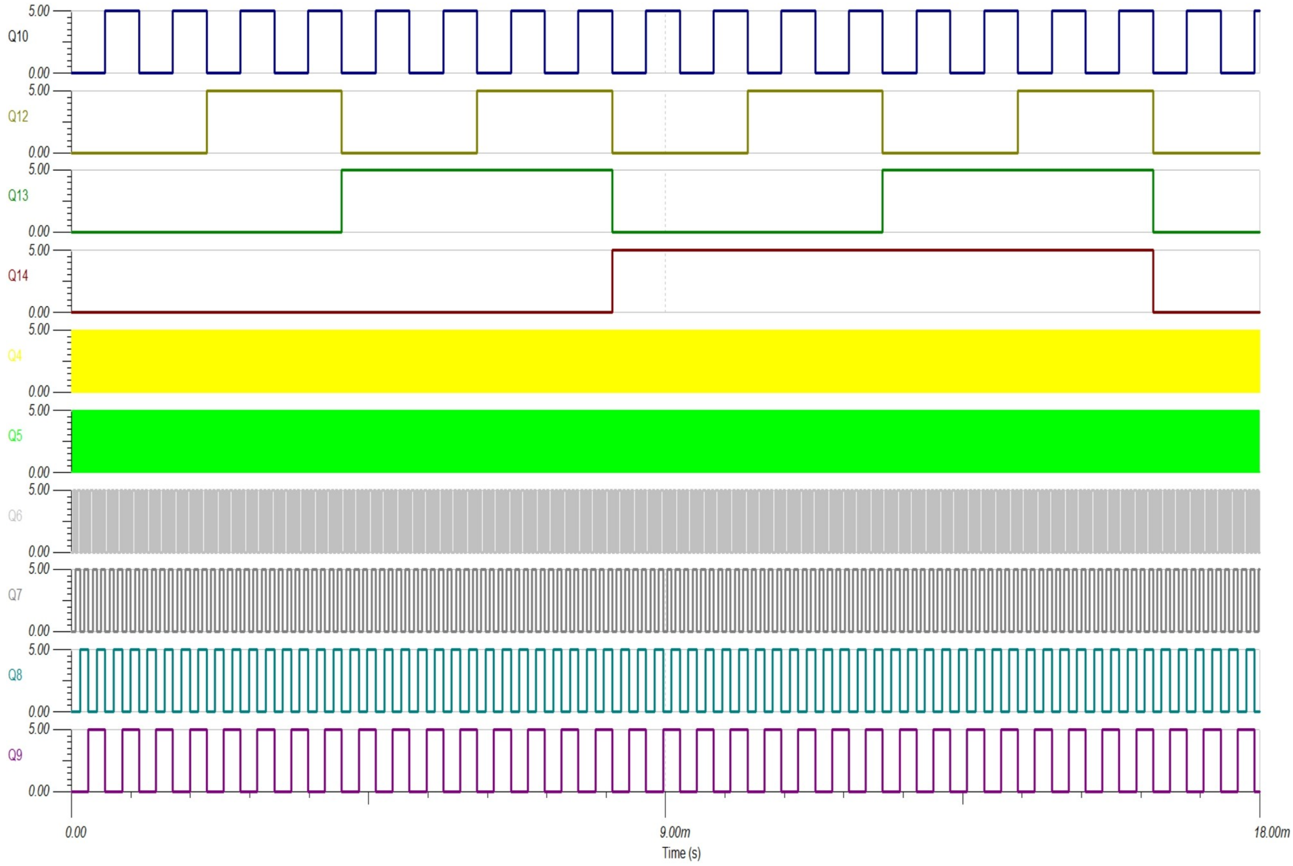
Timing diagram



The oscillator may be replaced by an external clock signal at input CLKI. In this case, keep the oscillator pins (CLKO1 and CLKO2) floating. The counter advances on the HIGH-to-LOW transition of CLKI.

Pinning





State changes of the Qn outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with CLKO2 of the 74HC4060.

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