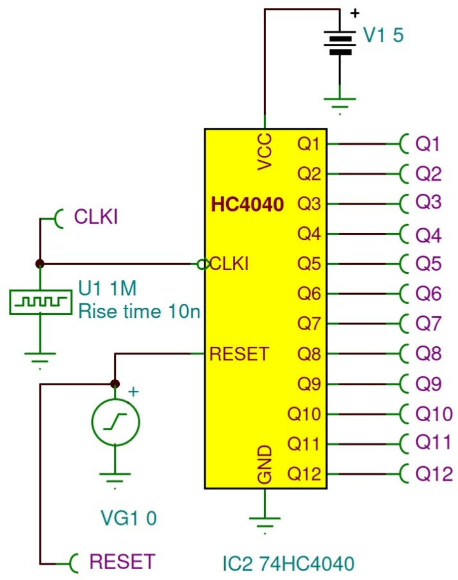
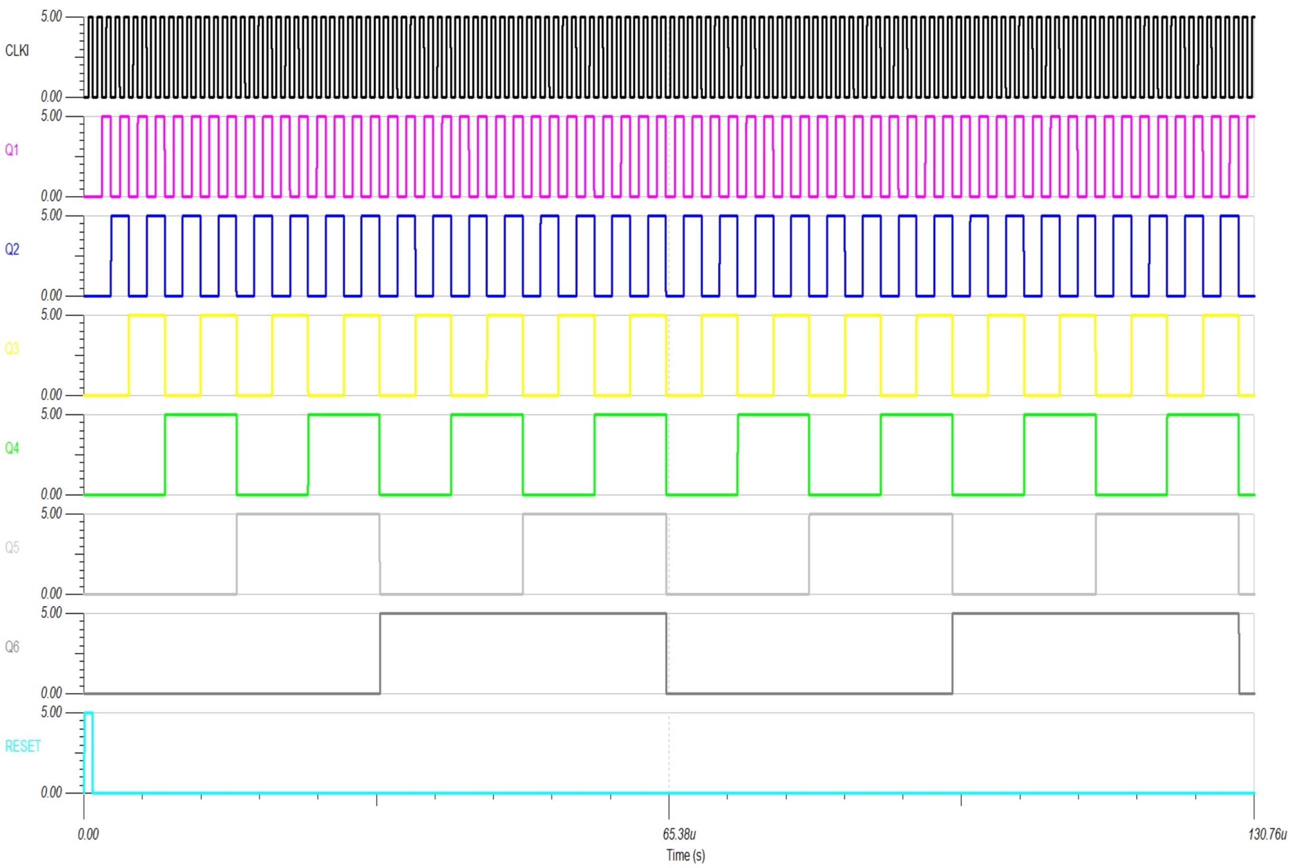
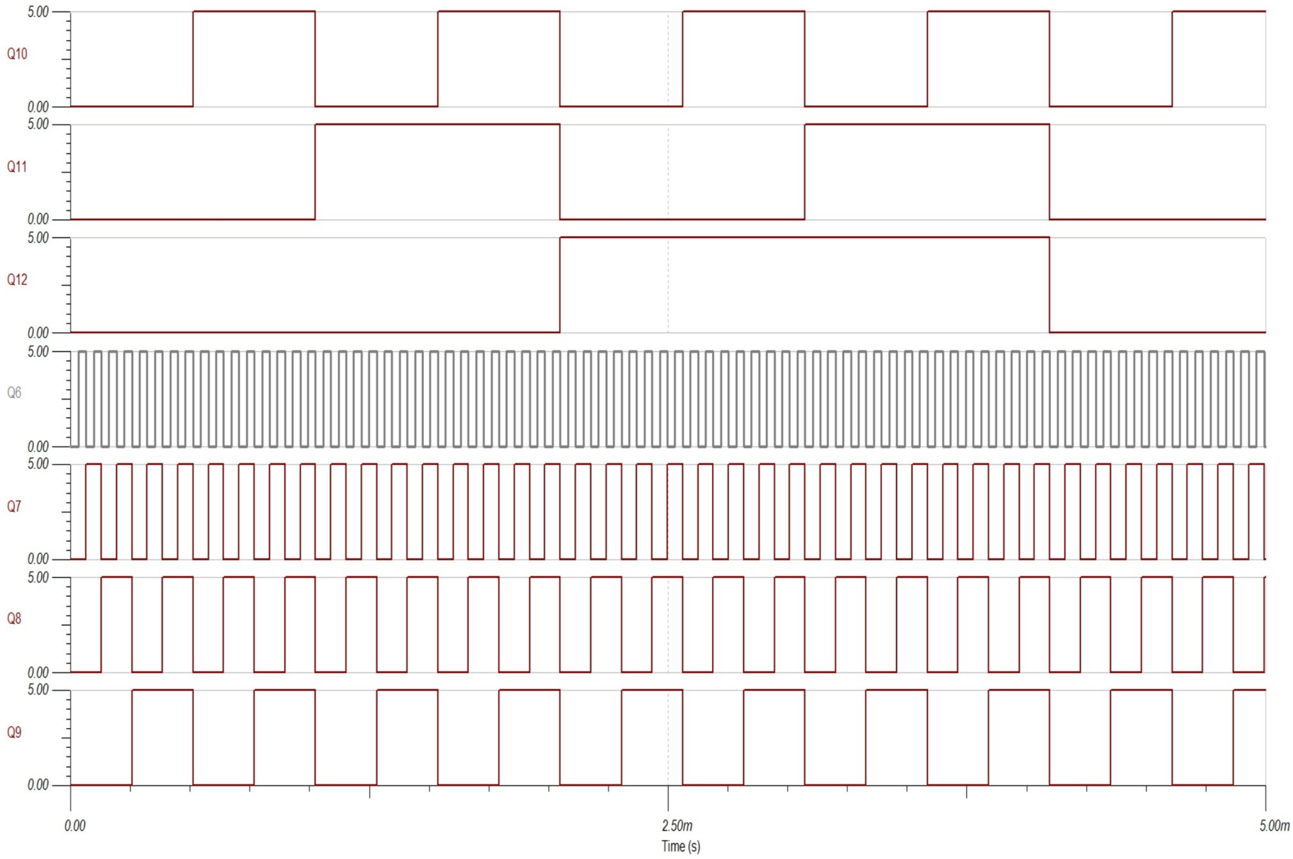
MM74HC4040 12-Stage Binary Counter Macro Model

Test Circuit



To enhance clarity, the complex diagrams are divided into two segments. The counter is driven by a 1 MHz clock signal, and the simulation duration is set to 5 ms. This timeframe ensures comprehensive validation of all output states. The outputs utilize analog CMOS technology, allowing for detailed analysis of their load behavior under simulated conditions.





State changes of the Qn outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with CLKI of the 74HC4040.
The signal propagation delay from CLKI to Q1 is 18 ns.
The propagation delay between consecutive outputs (Q_n to Q_{n+1}) is 9 ns.

Zabb Csaba